

Appln. No.: 10/772,079  
Amdt. Dated August 20, 2007

**Amendments to the Specification:**

On page 1 of the specification, please amend the first paragraph as follows:

The present invention is a continuation of Patent Application Serial Number 09/726,642, filed on November 30, 2000, now U.S. Patent No. 6,707,848, which is a continuation of 09/439,121, filed November 12, 1999, now U.S. Patent No. 6,201,831, which is a continuation-in-part of the following applications filed on August 09, 1999, commonly owned by the assignee of the present application, the contents of each of which are herein incorporated by reference: Serial Number 09/370,353, now U.S. Patent No. 6,226,332, entitled "Multi-Pair Transceiver Decoder System with Low Computation Slicer"; Serial Number 09/370,354, now U.S. Patent No. 6,249,544, entitled "System and Method for High-Speed Decoding and ISI Compensation in a Multi-Pair Transceiver System"; Serial Number 09/370,370, now U.S. Patent No. 6,253,345, entitled "System and Method for Trellis Decoding in a Multi-Pair Transceiver System"; and Serial Number 09/370,491, now U.S. Patent No. 6,525,904, entitled "High-Speed Decoder for a Multi-Pair Gigabit Transceiver".